ABSTRACT

An extending circuit for memory includes an output data effective signal generator for, when a status signal from a next-stage FIFO circuit represents a data writable state, asserting a write enable signal from the next-stage FIFO circuit, and enabling data to be written into the next-stage FIFO circuit. The extending circuit for memory also includes an internal FIFO write enable generator for receiving a status signal from the next-stage FIFO circuit, asserting an internal FIFO write enable signal, and enabling data to be written into an internal FIFO circuit of the extending circuit for memory, when the next-stage FIFO circuit is in a data unwritable state.